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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/567,851	10/06/2006	Jouni Kytomaa	59643.00669	7339

32294 7590 04/29/2009

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EXAMINER	
MITCHELL, DANIEL D	

ART UNIT	PAPER NUMBER
2419	

MAIL DATE	DELIVERY MODE
04/29/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/567,851	KYTOMAA ET AL.	
	Examiner	Art Unit	
	DANIEL MITCHELL	2419	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 January 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17; 35-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17; 35-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 February 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on January 8, 2009 has been entered. Claims 1-17 and 35-45 have been amended. Claims 18-34 are canceled. Claims 1-17 and 35-46 are still pending in this application, with claims 1, 35, and 46 being independent.

Response to Arguments

2. Applicant's arguments, see pg 13 lines 7-11, filed January 8, 2009, with respect to claims 1-45 have been fully considered and are persuasive. The rejections of 35 USC 102 for claims 1-45 has been withdrawn.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claim 35 is rejected under 35 U.S.C. 112, first paragraph, as a single means claim, i.e., where a means recitation does not appear in combination with another recited element of means. Applicant discloses a single processor is configured to perform to the entire functionality of the claims (i.e. queuing, scheduling, transferring,

etc..., of packets). (Refer MPEP 2164.08 (a) for rejection under 35 U.S.C. 112, first paragraph. In re Hyatt, 708 F.2d 712, 714-715, 218 USPQ 195, 197 (Fed. Cir. 1983)

5. Claim 46 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim independent claim 46 claims a computer readable storage medium, but the applicant fails to mention a computer readable storage medium in the specification. Furthermore computer readable storage medium is not defined in the specification.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

The USPTO "Interim Guidelines for Examination of Patent Applications for Patent Subject Matter Eligibility" (Official Gazette notice of 22 November 2005), Annex IV, reads as follows:

> Descriptive material can be characterized as either "functional descriptive material" or "nonfunctional descriptive material." In this context, "functional descriptive material" consists of data structures and computer programs which impart functionality when employed as a computer component. (The definition of "data structure" is "a physical or logical relationship among data elements, designed to support specific data manipulation functions." The New IEEE Standard Dictionary of Electrical and Electronics Terms 308 (5th ed. 1993).) "Nonfunctional descriptive material" includes but is not limited to music, literary works and a compilation or mere arrangement of data.

> When functional descriptive material is recorded on some computer-readable medium it becomes structurally and functionally interrelated to the medium and will be statutory in most cases since use of technology permits the function of the descriptive material to be realized. Compare In re Lowry, 32 F.3d 1579, 1583-84, 32 USPQ2d 1031, 1035 (Fed. Cir. 1994) (claim to data structure stored on a computer readable medium that increases computer efficiency held statutory) and Warmerdam, 33 F.3d at 1360-61, 31 USPQ2d at 1759 (claim to computer having a specific data structure stored in memory held statutory product-by-process claim) with Warmerdam, 33 F.3d at 1361, 31 USPQ2d at 1760 (claim to a data structure per se held nonstatutory).
>
> In contrast, a claimed computer-readable medium encoded with a computer program is a computer element which defines structural and functional interrelationships between the computer program and the rest of the computer which permit the computer program's functionality to be realized, and is thus statutory. See Lowry, 32 F.3d at 1583-84, 32 USPQ2d at 1035.

Claim(s) **[46]** is/are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter as follows. Claim **[46]** defines a **[a computer readable storage medium]** embodying functional descriptive material. However, the claim does not define a computer-readable medium or memory and is thus non-statutory for that reason (i.e., "When functional descriptive material is recorded on some computer-readable medium it becomes structurally and functionally interrelated to the medium and will be statutory in most cases since use of technology permits the function of the descriptive material to be realized" – Guidelines Annex IV). That is, the scope of the presently claimed **[a computer readable storage medium]** can range from paper on which the program is written, to a program simply contemplated and memorized by a person.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-17 and 35-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Olsen et al. (US 2005/0249220 A1), hereinafter referred as Olsen in view of Galbi et al (US Publication No. 20040202192 A9), hereinafter referred as Galbi in further view of Tuck et al. (US Patent No. 6,738,378 B2), hereinafter referred as Tuck.

Regarding claim 1, Olsen discloses a method: allocating each received packet to at least one arrival queue **(fig. 3 and par. 25 teaches inputting received data into an arrival queue)**; dropping said packet **(par. 24 teaches a policer for dropping packets prior to queuing)**; scheduling packets from the arrival queue to at least one transfer queue **(fig. 3 and par. 51 teaches after processing the packets, transferring packets to memory which is interpreted as a transfer queue).**

However Olsen does not expressly disclose generating an interrupt; responsive to receipt of an interrupt, allocating the packet from said transfer queue to one of a plurality of processor queues; placing the packet in the allocated processor queue and scheduling packets from the processor queues to be processed.

Galbi discloses in **par. 33** a memory 103 for storing packets, where the memory is equivalent to the memory disclosed in **par. 51 and fig. 6** of the primary reference. Galbi discloses in **par. 33-34** generating a request, interpreted as an interrupt, upon receipt of the transfer of data to memory (transfer queue). Galbi discloses in **par. 33** a memory (transfer queue) for receiving data. Galbi discloses in **par. 34** creating work queues, interpreted as processor queues, so processor 104 can process packets. Galbi discloses in **par. 34** allocating packets to be processed to the work queues.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Olsen to include utilizing the transfer queue to transfer data to the processor. One would be motivated as such in order conserver core processor capacity by offloading tasks **par. 34.**

However Olsen and Galbi do not expressly disclose if said queue is not full, otherwise dropping said packet.

Tuck discloses in **col. 6 lines 47-65** that packets are added to queues if the queue is not full, otherwise the packet is dropped.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Olsen in view of Olsen to include dropping packets when queues become full. One would be motivated as such in order allow the CPU to process data according to the priority during the presence of an overload condition **col. 2 lines 20-25.**

Regarding claim 2, Olsen discloses in **fig. 6 and par. 51** a plurality of linecards, interpreted as devices, for receiving packets.

Regarding claim 3, Olsen discloses in **fig. 3** wherein at least one device has a plurality of arrival queues **(par. 10 and 22-23 and fig. 3** teaches various sets of queues 40 where it is interpreted a device includes a set of queues 40).

Regarding claim 4, Olsen discloses in **par. 23 and 32** wherein each arrival queue is associated with a traffic class, each packet being allocated to the at least one queue in accordance with the traffic class of each packet **par. 23 teaches classifying packets based on information stored in the header of each packet and par. 32 teaches each queue is associated with a class.**

Regarding claim 5, Olsen discloses in **par. 23, 32** wherein the traffic class is priority information embedded in the each packet **(par. 23, 32 teaches a packet header including classification information and priority information)**.

Regarding claim 6, Olsen discloses a (memory) transfer queue **fig. 6 element 68. However Olsen does not expressly discloses a plurality of transfer queues.**

Galbi discloses in **par. 33** a memory 103 including multiple transfer queues **(par. 33 teaches the memory includes a plurality of buffers).**

See similar motivation as claim 1.

Regarding claim 7, Olsen discloses wherein the number of transfer queues is less than the number of arrival queues **(fig. 3** teaches a plurality of arrival queues 40 and **fig. 6** single transfer queue 68**).**

Regarding claim 8, Olsen discloses wherein the scheduling of packets from the arrival queue to the transfer queue is dependent upon one or more of: the traffic profile **(par. 30 teaches scheduling the de-queuing of packets is dependent upon bandwidth, which is a traffic profile).**

Regarding claim 9, **Olson does not expressly disclose wherein the transfer queue comprises a device level transfer queue and a processor level transfer queue, wherein the device level transfer queue receives packets from the arrival queue, and the processor level transfer queue receives packets from the device level transfer queue.**

Galbi discloses in **fig. 3.** a transfer queue consisting of transfer queues 314 and processor queues 312 where queue 314 receives data from the received data from the receiving interface 106 and processor queues 313 receive data from transfer queues 314 **(see also par. 45-47)**.

See similar motivation as claim 1.

Regarding claim 10, Olson **does not expressly disclose wherein packets are transferred to the processor level transfer queue from the device level transfer queue whenever there is space in the processor level transfer queue.**

Galbi discloses **par. 34** co-processor creates the queues by transferring packets to processor queues when space is available.

See similar motivation as claim 1.

Regarding claim 11, **Olson does not expressly disclose wherein packets are never dropped from the transfer queue.**

Galbi discloses in **par. 34** the co-processor stores data in a queue (memory).

See similar motivation as claim 1.

Regarding claim 12, Olsen discloses a processor 62 **fig. 6. However Olsen does not expressly disclose wherein the processor, processor queues exist that are associated with different priorities.**

Galbi discloses in **par. 34** teaches prioritized work queues that exist with in a processor.

See similar motivation as claim 1.

Regard claim 13, Olsen discloses in **par. 32** highest priority has the lowest latency. **However Olson does not expressly discloses the highest priority has the lowest drop probability.**

Tuck discloses in **col. 6 lines 47-65** that packets with the highest priority have the lowest drop probability.

See similar motivation as claim 1.

Regarding claim 14, Olsen discloses wherein responsive to receipt of the packet is removed from a transfer queue and classified **par. 32 receives the request and places packets in work queues based on priority.**

Regarding claim 15, Olsen discloses wherein the classification is based on a determination of priority **(par. 32 teaches determining a processing order based on priority and par. 34 teaches classifying packets into prioritized work queues)**.

Regarding claim 16, Olsen discloses wherein the packet is allocated to a processor queue in accordance with its classification of the packet **par. 32 teaches distributing packets to work queues based on priority**.

Regarding claim 17, **Olsen discloses does not expressly disclose wherein the packet is placed in the allocated processor queue if said queue is not full, otherwise the packet is dropped.**

Tuck discloses in **col. 6 lines 47-65** that packets are placed in processor queues when space is available, otherwise the packets are discarded.

See similar motivation as claim 1.

Regarding claim 35, Olsen discloses an apparatus, comprising: a processor (fig.6 processor 62, par. 50) configured to allocate a received packet to at least one arrival queue **(fig. 3 and par. 25 teaches inputting received data into an arrival queue)** wherein the processor is configured to dropping said packet **(par. 24 teaches a policer for dropping packets prior to queuing)**, wherein the processor is configured to schedule packets from the arrival queue to at least one transfer queue**(fig. 3 and par. 51 teaches after processing the packets, transferring packets to memory which is interpreted as a transfer queue).**

However Olsen does not expressly disclose the processor generating an interrupt; responsive to receipt of an interrupt, allocating the packet from said transfer queue to one of a plurality of processor queues; placing the packet in the allocated processor queue and scheduling packets from the processor queues to be processed.

Galbi discloses in **par. 33** a memory 103 for storing packets, where the memory is equivalent to the memory disclosed in **par. 51 and fig. 6** of the

primary reference. Galbi discloses in **par. 33-34** generating a request, interpreted as an interrupt, upon receipt of the transfer of data to memory (transfer queue). Galbi discloses in **par. 33** a memory (transfer queue) for receiving data. Galbi discloses in **par. 34** creating work queues, interpreted as processor queues, so processor 104 can process packets. Galbi discloses in **par. 34** allocating packets to be processed to the work queues.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Olsen to include utilizing the transfer queue to transfer data to the processor. One would be motivated as such in order conserver core processor capacity by offloading tasks **par. 34.**

However Olsen and Galbi do not expressly disclose if said queue is not full, otherwise dropping said packet.

Tuck discloses in **col. 6 lines 47-65** that packets are added to queues if the queue is not full, otherwise the packet is dropped.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Olsen in view of Olsen to include dropping packets when queues become full. One would be motivated as such in order allow the CPU to process data according to the priority during the presence of an overload condition **col. 2 lines 20-25.**

Regarding claim 36, Olsen discloses in **fig. 6 and par. 51** comprising a plurality of arrival queues.

Regarding claim 37, Olsen discloses in **par. 23 and 32** wherein in which each arrival queue is associated with a traffic class, each packet being allocated to the at least one queue by the processor in accordance with the traffic class of each packet **(par. 23 teaches classifying packets based on information stored in the header of each packet and par. 32 teaches each queue is associated with a class).**

Regarding claim 38, Olsen discloses a (memory) transfer queue **fig. 6 element 68. However Olsen does not expressly discloses a plurality of transfer queues.**

Galbi discloses in **par. 33** a memory 103 including multiple transfer queues **(par. 33 teaches the memory includes a plurality of buffers).**

See similar motivation as claim 35

Regarding claim 39, **Olson does not expressly disclose wherein the transfer queue comprises a device level transfer queue and a processor level transfer queue, wherein the device level transfer queue receives packets from the arrival queue, and the processor level transfer queue receives packets from the device level transfer queue.**

Galbi discloses in **fig. 3.** a transfer queue consisting of transfer queues 314 and processor queues 312 where queue 314 receives data from the received data from the receiving interface 106 and processor queues 313 receive data from transfer queues 314 **(see also par. 45-47)**.

See similar motivation as claim 35.

Regarding claim 40, Olson **does not expressly disclose wherein packets are transferred to the processor level transfer queue from the device level transfer queue whenever there is space in the processor level transfer queue.**

Galbi discloses **par. 34** co-processor creates the queues by transferring packets to processor queues when space is available.

See similar motivation as claim 35.

Regarding claim 41, **Olson does not expressly disclose wherein packets are never dropped from the transfer queue.**

Galbi discloses in **par. 34** the co-processor stores data in a queue (memory).

See similar motivation as claim 35.

Regarding claim 42, Olsen discloses a processor 62 **fig. 6. However Olsen does not expressly disclose wherein the processor, processor queues exist that are associated with different priorities.**

Galbi discloses in **par. 34** teaches prioritized work queues that exist with in a processor.

See similar motivation as claim 35.

Regarding claim 43, Olsen discloses wherein responsive to receipt of the interrupt the packet is removed from a transfer queue and classified **par. 32 receives the request (interrupt) and places packets in work queues based on priority.**

Regarding claim 44, Olsen discloses wherein the packet is allocated to a processor queue in accordance with its classification of the packet **par. 32 teaches distributing packets to work queues based on priority**.

Regarding claim 45, **Olsen discloses does not expressly disclose wherein the packet is placed in the allocated processor queue if said queue is not full, otherwise the packet is dropped.**

Tuck discloses in **col. 6 lines 47-65** that packets are placed in processor queues when space is available, otherwise the packets are discarded.

See similar motivation as claim 35.

Regarding claim 46, Olsen discloses a computer-readable storage medium **par. 50** encoded with instructions that, when executed on a computer, perform a process, the process comprising: allocating each received packet to at least one arrival queue **(fig. 3 and par. 25 teaches inputting received data into an arrival queue)**; dropping said packet **(par. 24 teaches a policer for dropping packets prior to queuing)**; scheduling packets from the arrival queue to at least one transfer queue **(fig. 3 and par. 51 teaches after processing the packets, transferring packets to memory which is interpreted as a transfer queue).**

However Olsen does not expressly disclose generating an interrupt; responsive to receipt of an interrupt, allocating the packet from said transfer queue to one of a plurality of processor queues; placing the packet in the allocated processor queue and scheduling packets from the processor queues to be processed.

Galbi discloses in **par. 33** a memory 103 for storing packets, where the memory is equivalent to the memory disclosed in **par. 51 and fig. 6** of the primary reference. Galbi discloses in **par. 33-34** generating a request, interpreted as an interrupt, upon receipt of the transfer of data to memory (transfer queue). Galbi discloses in **par. 33** a memory (transfer queue) for receiving data. Galbi discloses in **par. 34** creating work queues, interpreted as processor queues, so

processor 104 can process packets. Galbi discloses in **par. 34** allocating packets to be processed to the work queues.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Olsen to include utilizing the transfer queue to transfer data to the processor. One would be motivated as such in order conserver core processor capacity by offloading tasks **par. 34.**

However Olsen and Galbi do not expressly disclose if said queue is not full, otherwise dropping said packet.

Tuck discloses in **col. 6 lines 47-65** that packets are added to queues if the queue is not full, otherwise the packet is dropped.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Olsen in view of Olsen to include dropping packets when queues become full. One would be motivated as such in order allow the CPU to process data according to the priority during the presence of an overload condition **col. 2 lines 20-25.**

Conclusion

8. Any response to this action should be **faxed** to (571) 173-8300 or **mailed** to:

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Hand delivered responses should be brought to:
Customer Service Window

Randolph Building
401 Dulany Street
Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANIEL MITCHELL whose telephone number is (571)270-5307. The examiner can normally be reached on Monday - Friday 8:00 am - 5:00 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chirag G. Shah can be reached on 571-272-3144. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/D. M./
Examiner, Art Unit 2419

/Chirag G Shah/

Supervisory Patent Examiner, Art Unit 2419